Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Third Semester

Information Technology

CS3351- Digital Principles and Computer Organization

(Common to Computer science and Engineering & Artificial intelligence and Data Science)

Regulations – 2021

Duration: 3 Hrs. *Maximum: 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Find the sum and carry expressions for half adder.	RE	1	2
2.	Evaluate the logic circuit of 2 bit comparator.	EV	1	2
3.	Outline the difference between a synchronous sequential circuit and an asynchronous sequential circuit.	UN	2	2
4.	List the characteristics of T flip flop.	RE	2	2
5.	Draw the stock diagram of Von – Neumann architecture.	RE	3	2
6.	Interpret the instruction set architecture.	UN	3	2
7.	Differentiate data hazards and control hazards.	RE	4	2
8.	What is pipelining?	RE	4	2
9.	Can a computer work without catch? Justify.	AN	5	2
10.	List the purpose of SATA?	UN	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Solve the following using K-map and boolean algebra: $F(A,B,C)=\sum m(1,3,5,7)$	AP	1	7
		ii	Simplify the function using multiplexer $f=\sum(0,1,3,4,8,9,15)$.	AP	1	6
			Or			
	b		Construct binary to octal decoder and octal to binary encoder with the help of circuit diagram.	AP	1	13
12.	a		Draw the logic circuits and the excitation tables for the T, JK, RS flip-flops.	UN	2	13
			Or			
	b	i	Explain about shift register? Outline the design of a four-bit shift register with a diagram.	UN	2	7
		ii	Outline the Mealy model and Moore model of the sequential circuits with a diagram.	UN	2	6
13.	a		Describe any five addressing modes with example	UN	3	13
			Or			
	b		Explain in detail about memory location address and operations.	UN	3	13

14.	a	Describe the methods for avoiding the control hazards.	UN	4	13
		Or			
	b	Explain in detail about designing a control unit.	UN	4	13
15.	a	Explain how memory mapping techniques are useful for finding memory blocks in cache.	UN	5	13
		Or			
	b	Explain in detail about direct memory access with a neat diagram.	UN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Discuss the steps involved in the address translation of virtual memory with necessary block diagram.	UN	4	15
		Or			
	b	Explain the basic MIPS implementation with necessary multiplexer and control lines.	UN	4	15